A NEW 2-INCH DATA DISK SYSTEM WITH A HIGH TRANSFER RATE

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Introduction

Since the advent of IBM's first 8-inchflexible disk system in 1971, disks and drives have become increasingly smaller via the 5-inch to the 3.5-inch. This miniaturization has meant that various recording characteristics, such as data transfer rate, have become outmoded.

In 1984, the MAVICA (MAgnetic VIdeo CAmera) system based on a 2-inch floppy disk was agreed on as a world standard called VF (still Video Floppy) system by forty-three companies which organized the Electronic Still Camera Conference.

Last year, the conference agreed on a digital data recording format based on this same VF disk. We report here on this new 2-inch data recording system and its application.

Target Features for 2-inch Data Disk system

We wanted the new system to have the following features:

1. High data transfer rate
2. Powerful ECC (Error Correction Code)
3. High data capacity
4. Logical interface
5. VF system compatibility
6. Minimized reliance on mechanical accuracy by digital signal processing design

Our first target was to obtain a data transfer rate equivalent to that of a hard disk system. The weakest point of conventional floppy disk systems is their slow data transfer rate.

Our second target was the introduction of a powerful ECC. Reliability is more essential for consumer products than for office products, because consumers often subject equipment to rough handling. In addition, it is difficult to produce a defect-free magnetic recording medium for short-wave recording at a reasonable cost. The ECC compensates for rough handling and makes it possible to produce a highly reliable product with high productivity.

Our third target was to have a data capacity equivalent to that of a conventional floppy disk system in spite of our system's smaller size and single-side format.

Our fourth target was to have a black-box storage device. Although the system is complex, we wanted a simple logical interface.

Our fifth target was that the system be compatible with the VF format. The head-medium interface should be fixed at 3,600 r.p.m. for the 2-inch VF disk system. The system should be able to handle analogue still video, analogue audio, and digital data.

Our last target reflects a basic policy. Using digital signal processing techniques rather than high-accuracy mechanical parts means a drastic reduction in costs and dimensions.

Track Format

The VF system has 50 main tracks for video, audio, and digital data recording. The 2-inch Data Disk system uses the whole 50 tracks for digital data recording. Fig.1 shows an outline of the digital data track format.

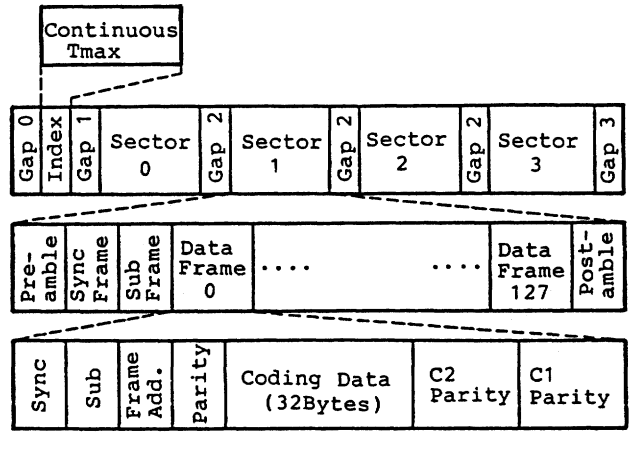

Fig.1 Track format of the digital data recording

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Each track has four physical sectors and one index area for sector positioning. Each physical sector has a 4-Kbyte data capacity. The relatively large size of the sectors means that burst error correction can be based on the collection of a large amount of interleaved data. Data in the sectors is broken up into 128 data frames. Each data frame consists of a 4-byte header, 32 bytes of information data, and two 4-byte blocks of Reed-Solomon redundancy code. The Sub-Code data is shuffled in each frame header, and forms four sets of the same 28-byte Sub-Code data.

Surface-recording

The 2-inch VF Disk uses high-Hc metal powder as magnetic recording particles whose coercivity is 1,300 Oersted. Since this is almost double the 3.5-inch disk's 720-Oersted coercivity, a maximum recording density of 51.2 Kbits/inch along the innermost track can be achieved. The diameter of the disk is a mere 47 mm (1.85 inch). Its total thickness is 40 um, including a 3-um thick magnetic layer coated on both sides of a polyester base film. Generally, it is difficult to achieve saturation magnetization in a thick magnetic layer with a narrow-gap read/write head in shortwave recording. We overcame this problem by employing a surface-recording technique as in Fig.2.

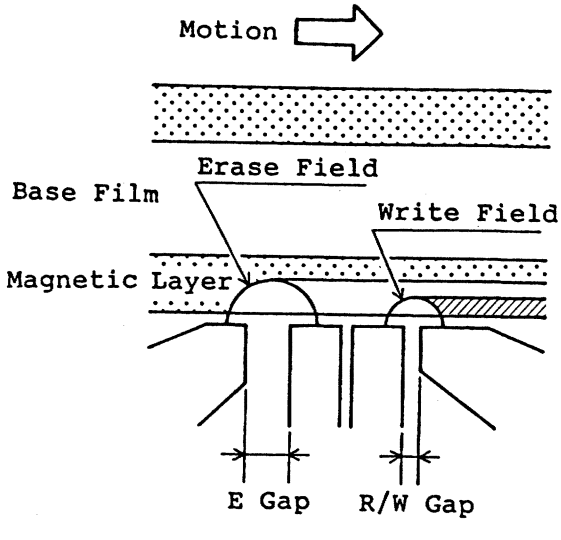

Fig.2 Surface-recording

Sufficient erasure is achieved by using a wide-gap leading-erase head. This technique allowed us to employ a coated medium with its attendant high productivity and high durability. We obtained forty million passes on the same track with less than 30% reduction in track amplitude.

A wide leading-erase head whose head gap is 140 um in width by 2.5 um in length is employed for both sector-erasing and side-trimming to maintain the medium's inter-changeability.

A R/W head whose head gap is 58 um in width by 0.4 um in length is combined with the above leading-erase head as in Fig.3.

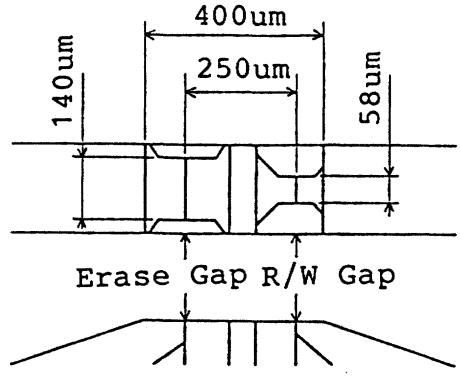

Fig.3 The leading-erase head

The center frequency of the FM video signal is about 7 MHz. This gives a 0.8 um recording wavelength on the innermost track. To maintain compatibility with video recording, we must use the same frequency range for digital data recording. For this reason, 7.16 MHz, which is double the NTSC color sub-carrier frequency, was chosen as the maximum recording frequency for digital data recording. This gives a 14.3 Mbps channel bit rate.

Generally speaking, the metal-in-gap head and the thin-film head are most suitable for use with a metal-coated medium. Unfortunately, these types of heads are still expensive. In order to employ the more readily available and less costly Ferrite head with surface recording instead of saturation recording, we choose a DC-suppressed 8-to-10 modulation method whose frequency range is concentrated near the shortwave region.

The parameters of this modulation method are:

Tw = Tmin = 0.8 T, Tmax = 3.2 T
(T: time interval of the source code)
| DSV | <= 3 (DSV: Digital Sum Value)

The conversion rules is the same as that for the DAT (Digital Audio Tape) system.

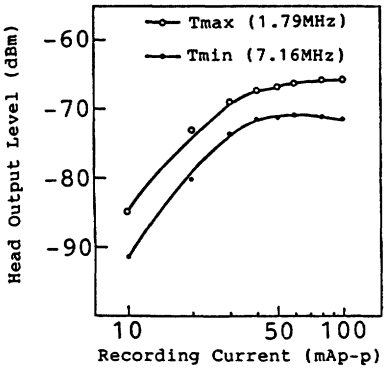

Fig.4 Input and output characteristics on the innermost track

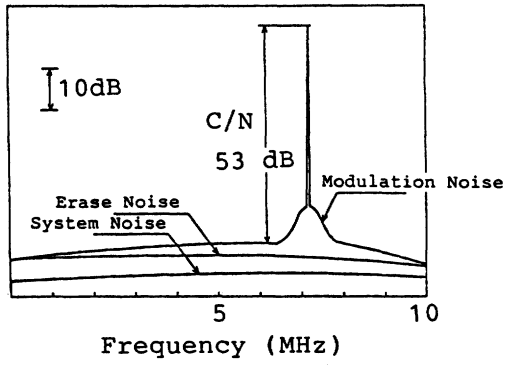

Fig.5 C/N ratio on the innermost track

The input and output characteristics on the innermost track using a ferrite head is shown in Fig.4. The C/N ratio on the innermost track is shown in Fig.5. We can realize slight magnetic saturation, but 53 dB of the C/N ratio is acceptable for digital data usage. For reference, we can get over 57 dB using a thin-film head, which is necessary for analogue video recording.

The obtained random byte error rate versus on track width is shown in Fig.6. We use as an acceptance criterion a random byte error rate of 10^{-4}, which is comparable to a C/N ratio of 41.5 dB, as in Fig.7. The inter-reration between the C/N ratio and on-track width is shown in Fig.8. This figure gives a minimum track width of approximately 20 um on the innermost track. The head-gap length versus the C/N ratio is shown in Fig.9. We determined that the R/W head-gap should be 0.42 um in length and 20 um in depth.

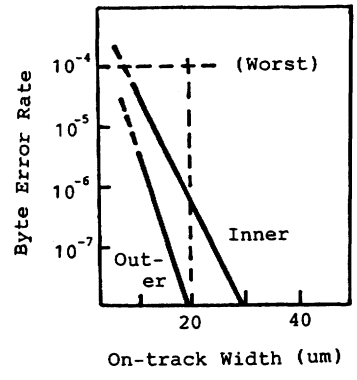

Fig.6 Random byte error rate vs. on-track width

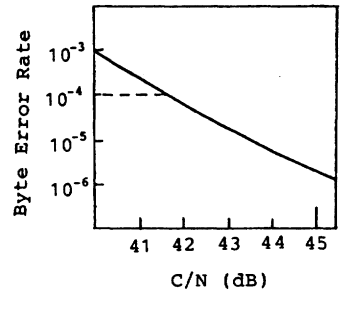

Fig.7 Random byte error rate vs. C/N ratio

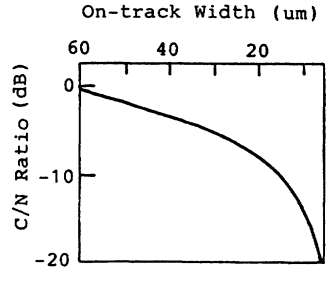

Fig.8 C/N ratio vs. on-track width

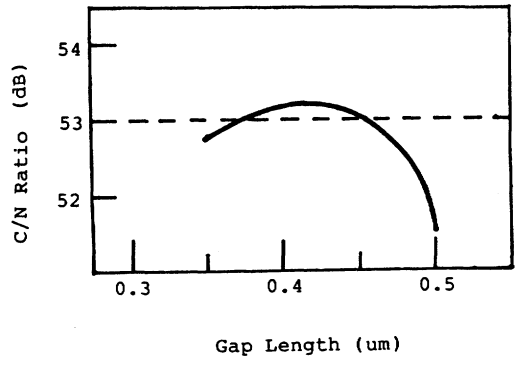

Fig.9 C/N ratio vs. R/W head gap length

Data Separator

A high-speed 14.3 Mbits/sec data separator has been achieved by using 8mm-VCR PCM recording technology. This data rate is almost double that of the hard disk drive. The embedded harmonized VFO locks into double the 7.16 MHz frequency of Tmin. The equalizer is employed for accurate data separation. The structure of the data separator is shown in Fig.10 .

At the start of data separation, a reproduced signal from the magnetic head whose signal level is about -70 dBm (0 dBm : 1 mW/ 50 ohms) is amplified by a head amplifier whose noise level is less than -130 dBm (Bw = 10 KHz). Phase linearity is necessary up to 10 MHz. An 8-mm VCR's RF amplifier was modified for this purpose.

The front equalizer is composed of differential and integral function units. The main role of this equalizer is to reproduce the amplitude component. The integral circuit compensates the differentialized waveform produced by magnetic recording. To generate an ideal waveform, the inverted differential signal is added.

The rear equalizer prevents total phase shift. The output signal from the front equalizer has a non-linear phase characteristic. A secondorder active low-pass filter tuned in an underdumping manner is employed to maintain phase linearity. This filter also suppresses undesirable high-frequency noise components.

The obtained eye-pattern at this point on the innermost track is shown in Fig.11. A 10^{-5} byte error rate on the innermost track, whose width was reduced to one-third of the nominal 58 um width, was obtained.

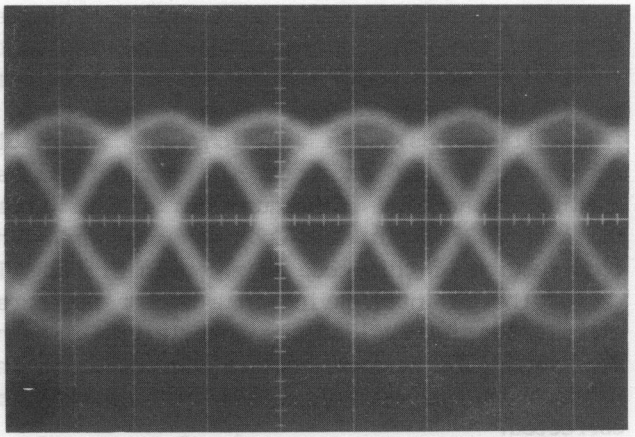

Fig.11 The eye-pattern on the innermost track

Error Detection and Correction

An improved CIRC (Cross Interleaved Reed-Solomon Code) was employed for this system. The two interleaved codes are C1 (41,37,5) and C2 (36, 32,5), both over $GF(2^8)$ in each sector. This kind of code is well known from the audio Compact Disc.

In constructing of the error correction code, we had to consider two types of errors. The first is random errors caused by mis-tracking, noise, azimuth-loss and head-medium wearing. The second is burst errors caused by dropouts, electro-magnetic noise, physical shocks, and servo slipping of the spindle motor. We had to select an ECC which is capable of dealing with both types of errors. To determine the optimum distance for each code, we also had to consider the total hardware size

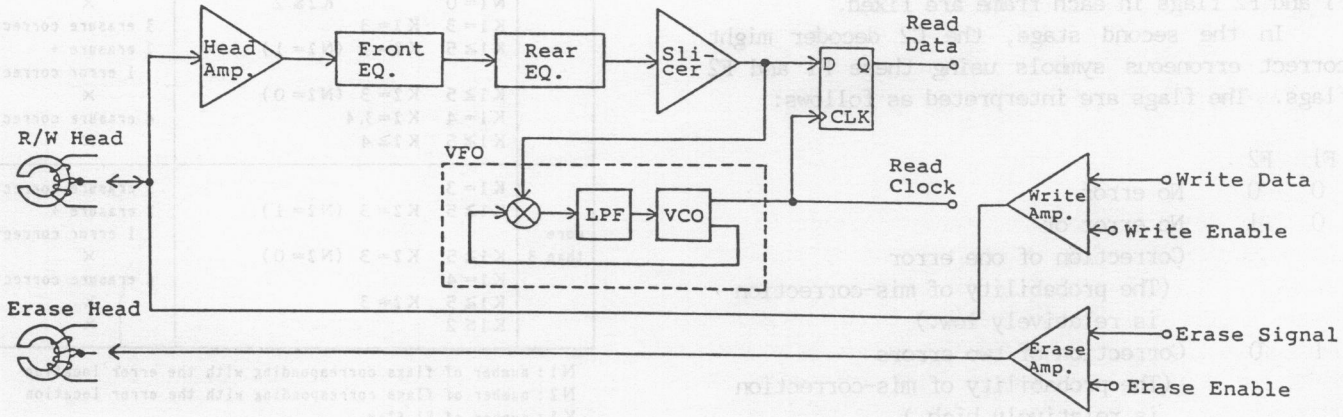

Fig.10 Block diagram of the data separator

required to achieve encodind/decording. We set ourselves the target of a single-chip disk controller LSI which would include all ECC functions, and the encode/decode time had to be reduced to a few milliseconds. In addition, the acceptable redundancy for ECC is about 20% of the total recording capacity. Consequently, a CIRC whose distance is five in each code was employed. The construction of this code is shown in Fig.12. To extend the C2 interleaving in a sector for burst errors, the interval of the interleaving is non-constant. The maximum erasure correction of the C2 code is four symbols, thus 14 frames can be corrected.

bursts occupying

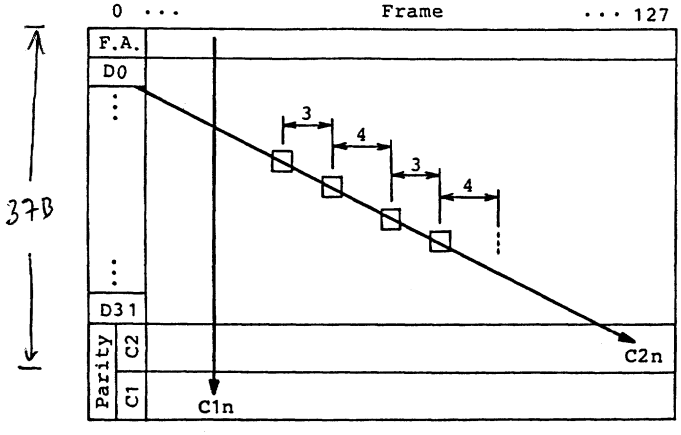

Fig.12 The construction of the ECC

The F1 and F2 flags are employed as the error probability pointers to prevent mis-correction. The flag strategy is as follows.

In the first stage, F1 and F2 flags are set in the uncorrectable case in the C1 decoder. The F1 flag is also set in the case of the two-error correction. At the end of the C1 decording, all F1 and F2 flags in each frame are fixed.

In the second stage, the C2 decoder might correct erroneous symbols using these F1 and F2 flags. The flags are interpreted as follows:

F1	F2	
0	0	No error
0	1	No error or Correction of one error (The probability of mis-correction is relatively low.)
1	0	Correction of two errors (The probability of mis-correction is relatively high.)
1	1	Un-correctable

The detailed algorithm of the C2 decording is shown in Table I. K1 and K2 give the total number of F1 and F2 flags in each frame. N1 and N2 give the total number of error location which reproduce C2 decording same location addressed by F1 and F2 flags. The ability to correct random errors of this strategy is shown in Fig.13.

Thus error-free reading is possible even if a burst error up to 2.43 mm long occurs in each sector on the innermost track or if the random error rate falls to 10^{-3} SER.

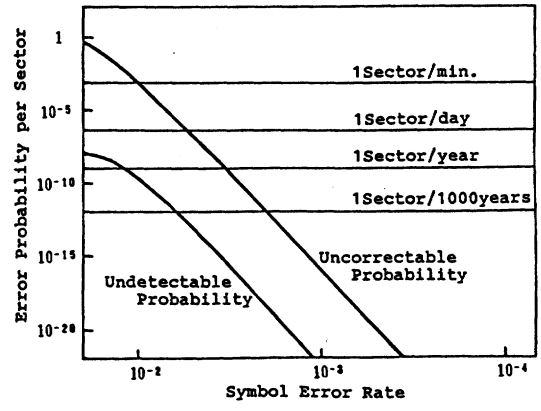

Fig.13 The ability to correct random byte errors

error	flag condition	operate
0	–	no correct
1	N2=1 N2=0 K2≦3 N2=0 K2≧4	1 error correct 1 error correct ×
2	N1=2 N2=2 K2=2 N1=2 N2=1 K2≦2 N1=2 N2=0 K2=0 N1=2 N2=0 K1≦4 K2=1,2 N1=2 N2=0 K1≧5 K2=1,2 N1=1 K1≦3 K2≦2 N1=1 K1≧4 K2≦2 N1=0 K2≦2 K1=3 K2=3 K1≧5 K2=3 (N2=1) K1≧5 K2=3 (N2=0) K1=4 K2=3,4 K1≧5 K2≧4	2 error correct 2 error correct 2 error correct 2 error correct × 2 error correct × × 3 erasure correct 2 erasure + 1 error correct × 4 erasure correct ×
more than 3	K1=3 K1≧5 K2=3 (N2=1) K1≧5 K2=3 (N2=0) K1=4 K1≧5 K2≠3 K1≦2	3 erasure correct 2 erasure + 1 error correct × 4 erasure correct × ×

N1: number of flags corresponding with the error location
N2: number of flags corresponding with the error location
K1: number of F1 flag
K2: number of F2 flag
× : uncorrectable

Table I Detailed algorithm of the C2 decoding

Advanced Disk Controller (ADC)

A disk controller LSI called the ADC which includes all digital signal processing circuits for this system has been developed. The ADC has four main blocks: Formatter, Deformatter, ECC and FDC. These blocks are connected by the internal bus as in Fig.14. An external 8-Kbyte static RAM for interleaving and deinterleaving is employed. This memory also acts as as a buffer memory, so the data transfer between the host system and disk drive is independent of the medium's rotational speed. This buffer memory can use as a 4-Kbyte disk cache memory. Therefore, we introduced a logical sector concept in which logical sectors can be used as 256, 512, or 4,096 bytes in this system.

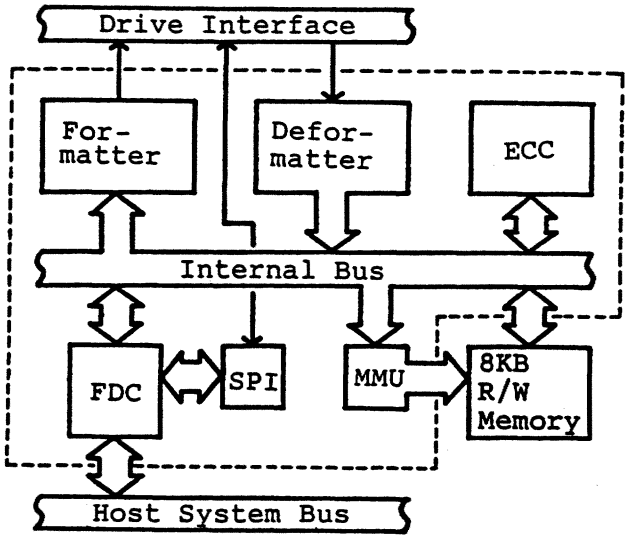

Fig.14 Block diagram of the ADC

The Formatter organizes sector data according to the track format from the contents of the RAM. The header data is automatically added to each frame, and data shuffling is carried out by the MMU (Memory Managing Unit). 8-to-10 modulation, parallel-to-serial conversion, and NRZI modulation are executed.

The Deformatter re-stores reproduced data on the RAM in the order of their address. This is different from the conventional floppy disk system in that the reproduced information is allowed to include some erroneous information. The sync detecting must be enhanced, because it is difficult to store data accurately on the RAM. We use Sync Frame and frame address for this purpose. Sync Frame is valid for sync slipping on the front portion of the sector caused by random errors. The mixture of random errors and burst errors causes a sharp reduction of the error-correction capability. The structure of the Sync Frame is as in Fig.15

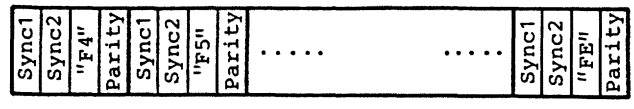

Fig.15 Structure of the Sync Frame

There are eleven sets of sync prediction signals whose length is four bytes each. Each four bytes includes double-sync and FPS (Frame Pre-Sync) and their parity. The value of the FPS starts from "F4" (" " means hexadecimal value) and ends at "FE". These continuous numbers will link to "FF", which is the frame number of the next Sub Frame. This "FF" hands its value to the frame counter for the Data Frame whose frame number starts from "00". The FPS is used to certify the frame counter. To prevent mis-detection, double-sync is employed. The value of each FPS is checked and applied as frame address if suitable.

The block diagram of the Deformatter is shown in Fig.16. Channel data is checked in 70 nsec cycles to determine sync or double-sync timing, and demodulated by the sub 10-to-8 demodulator to a byte value. The certificated header produces the final sync timing, and 10-to-8 demodulation is achieved.

Error correction and detection are achieved by using an optimized microprogram-controlled processor. Fig.17 shows the structure of the ECC block consisting of GLU (Galois-field Logic Unit), syndrome generator, sequencer, location register, and flag counter. We employed pipe-line techniques in the GLU, MMU, and Instruction decorder to reduce calculation time. The decording time is 6.8

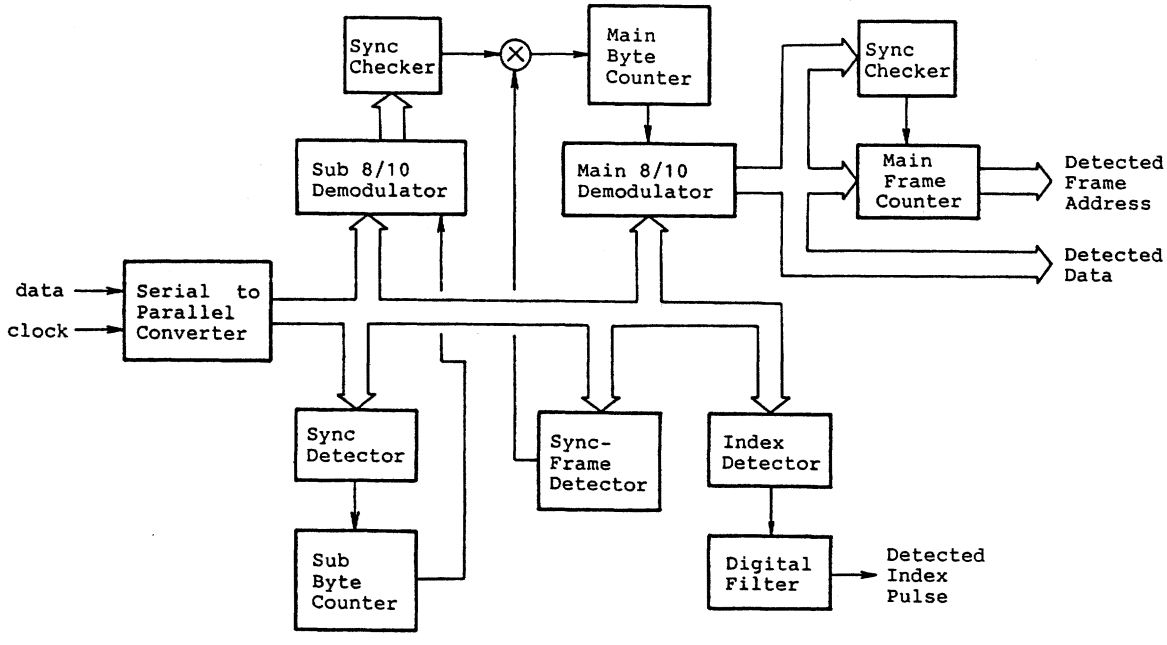

Fig.16 Block diagram of the deformatter

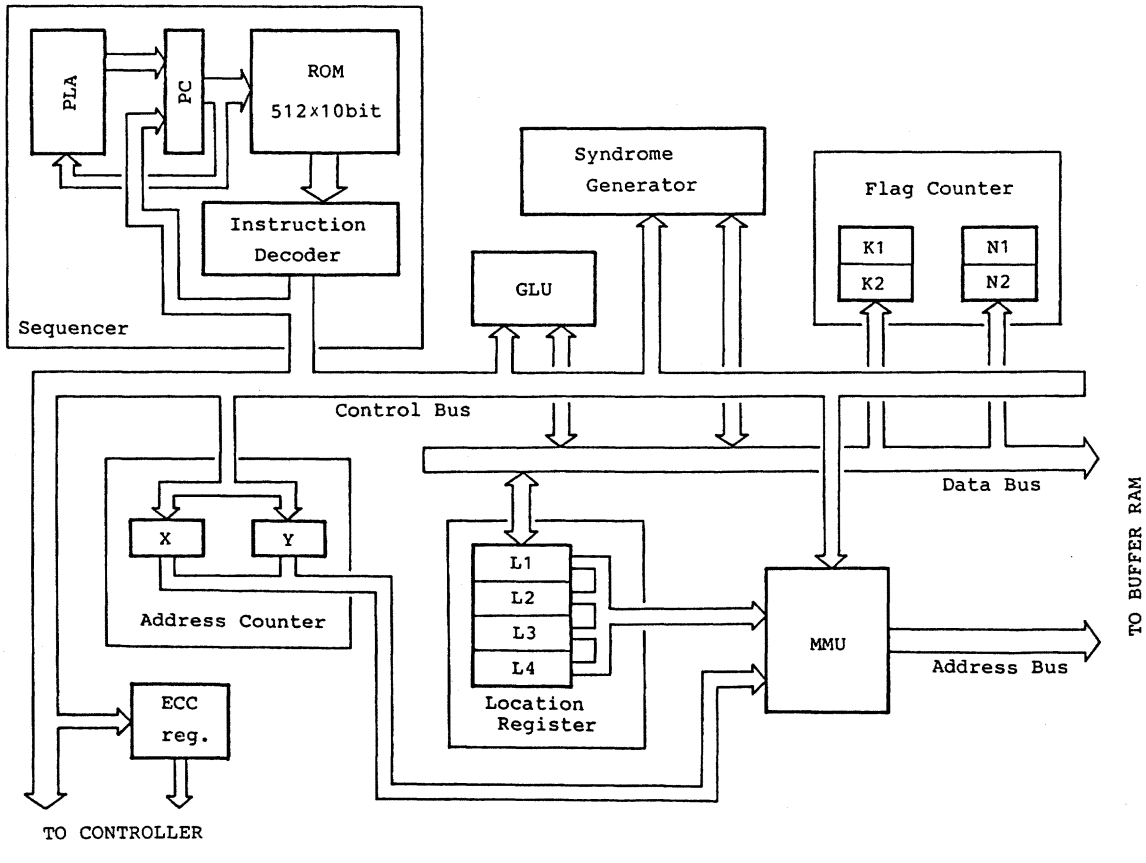

Fig.17 Block diagram of the ECC

msec for a normal pass up to 16.3 msec maximum for four-erasure correction. In the encording process, only 9.2 msec is necessary to form parity data on the buffer RAM. To reduce the size of the micro-program, this decoder also acts as an encoder. A PLA in the sequencer reduces the instruction data width. Many routines are packed as sub-routines for common usage in the C1 and C2 decoders. The FDC block uses the same sequencer. The size of the circuit of this block is about four thousand gates with MMU. The program flow is shown in Fig.18. We employed error-correction status flags in this system. These flags are shown in Table II.

The FDC block controls all the function blocks of this system. The FDC has an 8-bit data bus, address bus and control bus. Data transfer between the FDC and the disk drive is executed using two sets of serial lines. Each set of serial line corresponds to one drive unit.

value	C1 decode	C2 decode	total
00	no error	no error	no error
01	correct	no error	correct
10	correct or non-correct	correct	correct
11	correct or non-correct	non-correct	error

Table II ECC status flag

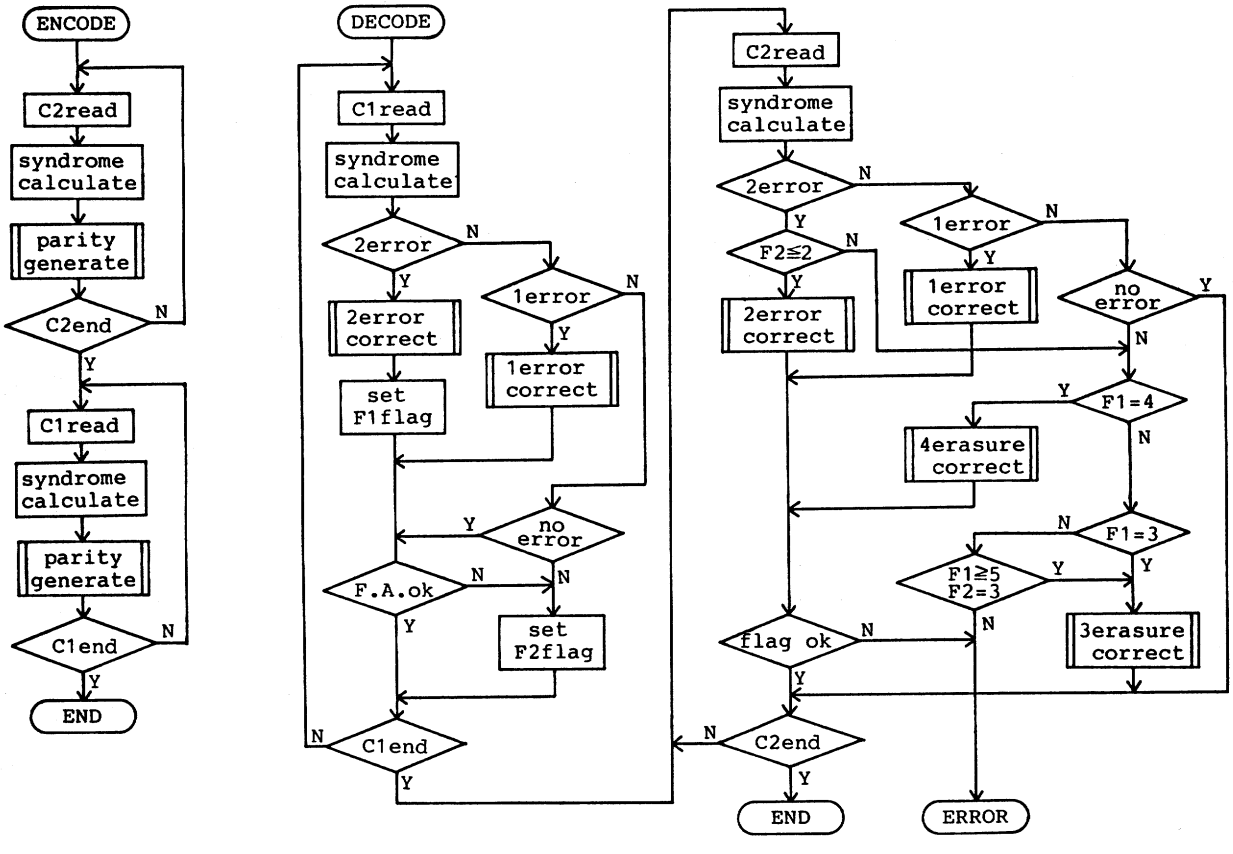

Fig.18 The flow-chart of the ECC

Fig.19 shows the bit assignment of the command register. A quite simple and logical one-byte command makes for easy operation in such a complicated system. Five executional bits are assigned as basic functions from bit 0 to bit 4. Each bit is combined or not combined to set to "1" with execution-enable bit 5.

For example, the following bit assignments cause:

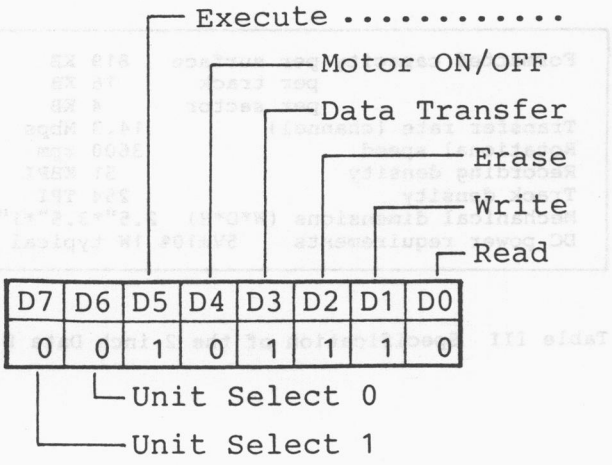

Fig.19 Bit assignment of the Command Register

1. Data transfer (host -> disk cache)
2. Spindle motor on
3. Seek
4. Calculate ECC parities
5. Make sector data
6. Erase
7. Write sector data
8. Receive executed status
9. Spindle motor off

A combination command is interpreted by the FDC block and resolved into each function. This system has a powerful hardware copy-protection mode. Two bytes of data in each sector written in an unwritable area are used for this purpose. In the data transfer mode, either DMA or non-DMA data transfer is selectable.

The ADC is implemented with 10,000 gates with ROMs and PLAs using 2-um CMOS standard-cell technology. Its die size is 9.3 mm by 8.8 mm and it is incorporated in an 80-pin flat plastic package. A photograph of the ADC is shown in Fig.20.

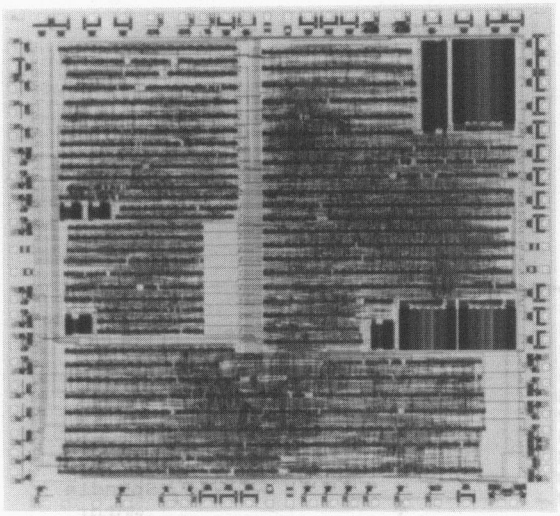

Fig.20 Die photograph of the ADC

Disk Drive

The head-medium interface is achieved using a combination of a solid air-pad and a penetrating head. The spacing between the R/W head-gap and medium's surface is kept less than 0.08 um, which enables very high-density magnetic recording. The rotational speed of the spindle motor, which is twelve times higher than that of the conventional floppy disk, has been achieved using low-inertia direct drive motor controlled by a software servo. We use an 8-bit microcomputer to achieve effective mechanical control as in Fig.21.

The main tasks of this microcomputer are:

1. Head positioning
2. Spindle-motor servo control
3. Switch management
4. Communication to/from the ADC

The software servo system has these advantages:

1. Adjustment-free production
2. Parts reduction
3. Modifiable and expandable
4. Single five-voltage power supply

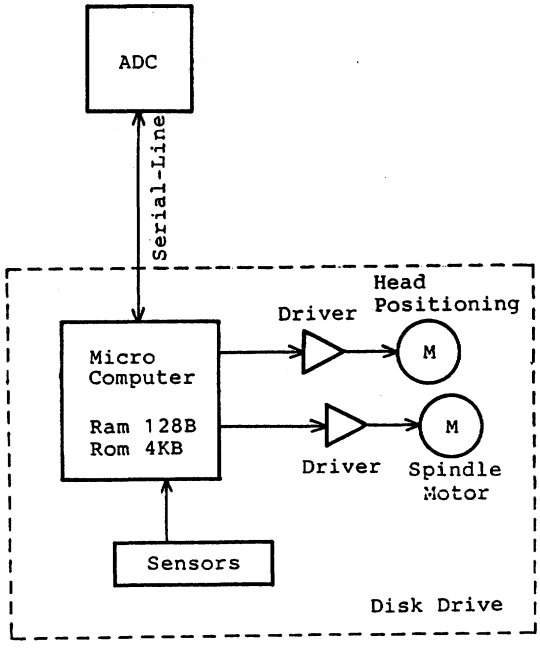

FIg.21 Block diagram of the mechanical control

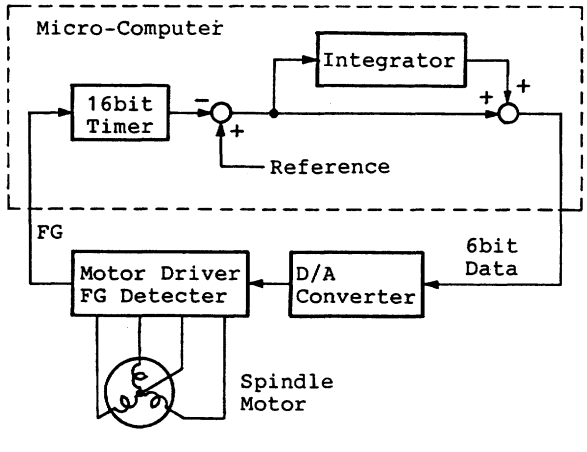

FIg.22 Block diagram of the software spindle motor servo system

The drive signal is produced by six-bit D/A converters. The input FG (Frequency Generator) pulses reproduced as back-EMF (Electro Motive Force) from the exciting coil of the motor are twenty-four pulses in one rotation. The block diagram of the speed servo is shown in Fig.22. The total program size of this microcomputer is 4-Kbyte with some debugger routines for mass-production.

The specifications of the 2-inch Data Disk drive are shown in Table III.

Formatted capacity	per surface	819 KB
	per track	16 KB
	per sector	4 KB
Transfer rate (channel)		14.3 Mbps
Rotational speed		3600 rpm
Recording density		51 KBPI
Track density		254 TPI
Mechanical dimensions (W*D*H)		2.5"*3.5"*1"
DC power requirements		5V±10% 1W typical

Table III Specification of the 2-inch Data Disk

Conclusion

A high-speed 2-inch Data Disk system which has a fast 14.3 Mbps data transfer rate has been developed. This system also has a powerful ECC called CIRC which is valid for both random and burst errors. Error-free data reading is possible even if the random byte error rate falls to 10^{-3}, or the burst error is up to 2.43 mm long in each sector. The obtained formatted capacity is 0.819 Mbytes with a single-side usage. It incorporates a newly designed disk controller LSI called the ADC.

Acknowledgements

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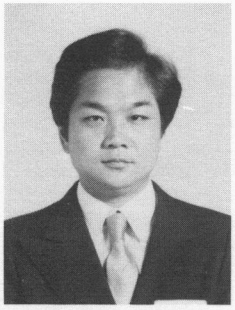
Biography



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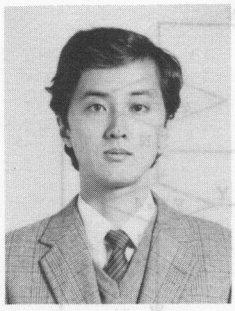

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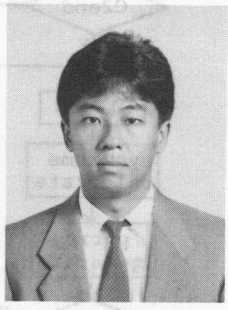

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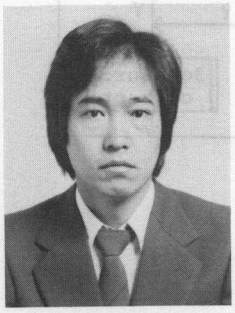

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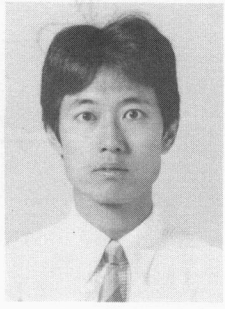

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